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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/682,054	10/09/2003	Kim Hwee Tan	APS03-002	8182

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EXAMINER	
PHAM, THANH V	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

KA

Office Action Summary	Application No.	Applicant(s)	
	10/682,054	TAN ET AL.	
	Examiner	Art Unit	
	Thanh V. Pham	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,16,19-35,38,41-58,61 and 64-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13, 16, 19-35, 38, 41-58, 61, 64-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims **1, 46,** 69 and 71 are rejected under 35 U.S.C. 102(b) as being anticipated by Kondoh et al. US 5,448,114 (provided by applicant).

The Kondoh et al. reference discloses in fig. 19 prior art die 1 comprising a substrate and a pillar structure

> In this example, the processes as far as the formation of the barrier metal layer 42 are the same as those shown in fig. 17. Next, a resist patterning for plating is formed on the barrier metal layer 42 and then a pillar-shaped, high melting-point core layer 44 of copper or nickel is selectively formed by electroplating. Further, a solder layer 45 is formed on the core layer 44 using electroplating. By reflowing the solder layer, a bump is formed (col. 5, lines 14-24).

The prior art as recognized by Kondoh et al. clearly teach the same process as instant figs. 5-7. Further, in another passage, col. 10, lines 55-65, Kondoh et al. teach

> the effect of controlling the bump shape will be explained. The absorb distortions resulting from a difference in coefficient of thermal expansion, a tall cylindrical bump or a drum-shaped bump is ideal... when a solder bump is reflowed naturally, it is shaped like a symmetrical drum whose side portions bulge. The shape is determined by the volume of solder, the weight of the chip, and the shape and size of the wetted electrode portion. Thus, to make this shape into an ideal one, it is necessary to add improvements to the device and assembly processes or to provide a spacer.

Furthermore, in another passage, col. 12, lines 4- 22, Kondoh et al. teach

> In the assembly process of bonding the chip to the board, there are two methods: one is to bond them by one reflow connection and the other is to first reflow only

> the chip and shape bumps, and then reflow again for bonding. Although either method can be applied to the invention, there may be a case where an improvement must be added to a face-down bonding apparatus that mounts the chip on the board. Specifically, when reflow is performed before bonding as in the after method, it is difficult to cause the bump's height to coincide with the height of the mall member. For this reason, such an operation is necessary as applies pressure to the chip once to permit all the bumps and the wall member to come into contact with the board and then remove the pressure, in the former method however, such an operation is not necessary because the bumps and the wall member agree with each other in height. Yet, doing such an operation helps reduce the reject rate.

It is clearly from the teaching of the above two last extracted passages, the bumps formed in the first extracted passage, after reflowing only the chip and shaping the bumps, have the claimed bi-layer pillar structure with a lower lead-free portion and a coextensive upper solder material portion.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 2, 9, 11-13, 19 and **24**, 31, 33-35, 41 and 47, 54, 56-58, 64 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondoh et al. as applied to claims **1, 46,** 69 and 71 above, and further in view of the following reasons.

Re claims 1-2, 24 and 46-47, the Kondoh et al. reference discloses further a die and method of forming a die 1 comprising the steps: providing a substrate 1; and forming one or more pillar structures 3/4 over the substrate in a pattern; at least one of the one of the one or more pillar structures having a lower lead-free portion 53 and a coextensive upper solder material portion 54. Wherein the one or more pillar structures have a rectangular shape, a side of element 3 (or the square shape of element 4 is

considered as a special rectangular with the two consecutive equal sides) or round shape, col. 10, lines 57-58. *Re claims 9, 31 and 54*, the pillar structure pattern includes 2 rows and 2 columns, fig. 2. *Re claims 11-13, 33-35 and 56-58*, the one pillar structure 3 is wall-shaped pillar structure forming a square, fig. 2. *Re claims 19, 41 and 64*, a lower copper layer 53 and an overlying reflowed solder layer 54, the solder layer being comprised of 60 % tin and 40 % lead (col. 14, lines 16-33). *Re claims 69-71*, the lower lead-free portion 53 is comprised of copper (col. 14, lines 26 and 52).

The improvement of Kondoh et al. from two-layer pillar structure to three-layer pillar structure is to prevent "external force-caused distortion concentrates on the portion of the solder material surrounding the core" (col. 6, lines 12-14). However, the bi-layer pillar structure bumps 45, similar to the instant invention, is already an improvement in compared with the bumps 43 in fig. 17 (col. 5, lines 7-12). It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the bi-layer pillar structure bumps further characteristics/applications as recognized above by Kondoh et al. (while the pillar structure of the bumps are maintained at two-layer structures) because the further characteristics/applications would "provide a good moisture-proof" (col. 6, line 23) as taught by Kondoh et al.

5. Claims 3-8, 10, 16, 20-23 and 25-30, 32, 38, 42-45 and 48-53, 55, 61, 65-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondoh et al. as applied to claims **1**-2, 9, 11-13, 19 and **24**, 31, 33-35, 41 and **46**-47, 54, 56-58, 64 and 69-71 above, and further in view of Lee et al. US 6,642,136 B1 and the following reasons.

The Kondoh et al. reference discloses substantially all of the invention. It discloses, though, "the bump 4 is approximately 100 micron square and 50 micron high, and the wall member 3 is approximately 300 micron wide and 50 micron high" (col. 9, lines 40-42), "the size of the chip is approximately 6 mm square and the number of pads is approximately 40; therefore, the contact area of the bump is approximately 0.4 mm^2 and that of the wall is approximately 4.0 mm^2", col. 10, lines 3-7, e.g. It does not disclose the claimed length, width, height and distance apart of each of the bumps nor the diameter of the sound pillar structure as claimed in claims 3-8, 10, 21-22 and 25-30, 32, 43-44 and 48-53, 55, 66-67. However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

Re claims 16, 38 and 61, the Kondoh et al. reference discloses (col. 14, line 52) "barrier layer 53 made of nickel, copper, or palladium" but does not state clear the lower portion comprising of copper coated with oxide, chromium or nickel. The Lee et al. reference discloses a lower lead free portion 54 of a solder bump made of copper coated with nickel 56 and covered with solder 58 (fig. 8). It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the lower lead-free portion of copper coated with nickel of Lee et al. because the structure and method of Lee et al. would provide the structure and method of Kondoh with "high-pillar solder bump that sustains a high stand-off of the complete solder bump while maintaining high bump reliability and minimizing damage caused by mismatching or thermal stress factors between the interfacing surface" (Lee et al.'s col. 2, lines 19-23).

Re claims 20, 42 and 65, the Kondoh et al. reference discloses the solder layer being comprised of 60 % tin and 40 % lead (col. 14, lines 28-29), "combination of the first supporting layer and second supporting layer is not restricted to the above combination" (col. 15, lines 1-6). Choice of the solder layer being consisting of about 63 % tin and 37 % lead or 100 % tin would have been a matter of routine optimization because the ratio of material in a layer are known to affect device properties and would depend on the desired device density on the finished wafer and the desired device characteristics. One of ordinary skill in the art would have been led to the recited ratio through routine experimentation to achieve desired deposition and reaction rates.

Re claims 23, 45 and 68, the Kondoh et al. reference discloses "when the semiconductor device is a high frequency element, using the electrode 7 as a ground

line provides a shielding effect" or "since the active area is isolated from the outside world by the chip itself, circuit board, and wall member, especially when the semiconductor device is a high-frequency element, the electrical shielding effect can be expected", col. 9, lines 27-29 and lines 50-53. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the shield of Kondoh et al. in Surface Acoustic Wave device and in MEM device because the shield would proved the Surface Acoustic Wave device or MEM device with proper shielding effect as taught by Kondoh et al.

Response to Arguments

6. Applicant's arguments filed 03/10/2006 have been fully considered but they are not persuasive.

7. Applicant's argument based on the added limitation of "after reflowing" is responded as in the above rejection. It is clear from the teaching of Kondoh et al. (the above extracted passages of col. 10, lines 55-65 and col. 12, lines 4- 22), the bumps formed after reflowing only the chip and shaping the bumps, have the claimed bi-layer pillar structure with a lower lead-free portion and a coextensive upper solder material portion. "When a solder bump is reflowed naturally, it is shaped like a symmetrical drum whose side portions bulge. The shape is determined by the volume of solder, the weight of the chip, and the shape and size of the wetted electrode portion".

8. The statement "before reflowing" in the previous office action relates to the second reflowing steps for bonding and should be read in the context of whole sentence

"In the assembly process of bonding the chip to the board, there are two methods: one is to bond them by one reflow connection and the other is to first reflow only the chip and shape bumps, and then reflow again for bonding". The claimed structure is held in between the two reflows.

9. Other arguments on dependent claims are the same as on the independent claims 1, 24 and 46 and are responded the same.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-Th (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVP

03/21/2006

George Fourson
Primary Examiner